Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-18. (cancelled)

19. (previously presented) A semiconductor device according to claim 22, further comprising:

a lowermost wiring layer nearest to the semiconductor substrate and provided below the first wiring layer; and

an uppermost wiring layer farthest from the semiconductor substrate and provided above the second wiring layer.

20. (previously presented) A semiconductor device according to claim 19, wherein a wiring pitch of the first wiring layer is greater than that of the second wiring layer.

21. (previously presented) A semiconductor device according to claim 19, wherein the first wiring layer is a layer on which a power source line is formed.

22. (previously presented) A semiconductor device comprising:

a semiconductor substrate;

a first wiring layer having a first thickness and provided above the semiconductor substrate; and

a second wiring layer having a second thickness thinner than the first thickness and provided above the first wiring layer,

wherein the first wiring layer comprises a first area having signal lines and a second area having power source lines, and a pitch of the power source lines is greater than that of the signal lines.

23. (previously presented) A semiconductor device according to claim 19, wherein the first wiring layer comprises a first area having signal lines and a second area having power source lines, and a width of each of the power sources lines is greater than that of the signal lines.

24. (previously presented) A semiconductor device according to claim 19, wherein the first wiring layer is substantially as thick as the uppermost wiring layer.

25. (previously presented) A semiconductor device according to claim 19, wherein the second wiring layer is substantially as thick as the lowermost wiring layer.

26. (previously presented) A semiconductor device according to claim 19, wherein all of the uppermost wiring layer, the lowermost wiring layer and the first and second wiring layers are metal layers.

27. (cancelled)

28. (previously presented) A semiconductor device according to claim 33, further comprising:

a lowermost wiring layer nearest to the semiconductor substrate and provided below the first wiring layer; and

an uppermost wiring layer farthest from the semiconductor substrate and provided above the second wiring layer.

29. (previously presented) A semiconductor device according to claim 28, wherein the first wiring layer is a layer on which a core power source line is formed.

30. (previously presented) A semiconductor device according to claim 28, wherein a wiring pitch of the first wiring layer is greater than that of the second wiring layer.

31. (previously presented) A semiconductor device according to claim 28, wherein the first wiring layer is substantially as thick as the uppermost wiring layer.

32. (previously presented) A semiconductor device according to claim 28, wherein the second wiring layer is substantially as thick as the lowermost wiring layer.

33. (previously presented) A semiconductor device comprising:

a semiconductor substrate;

an IP core area on the semiconductor substrate;

a peripheral area on the semiconductor substrate except for the IP core area;

a first wiring layer having a first thickness and provided above the semiconductor substrate in the IP core area; and

a second wiring layer having a second thickness smaller than the first thickness and provided above the first wiring layer in the IP core area,

wherein the first wiring layer comprises a first area having signal lines and a second area having power source lines, and a pitch of the power source lines is greater than that of the signal lines.

34. (previously presented) A semiconductor device according to claim 28, wherein the first wiring layer comprises a first area having signal lines and a second area having power source lines, and a width of each of the power source lines is greater than that of the signal lines.

35. (previously presented) A semiconductor device according to claim 28, wherein all of the uppermost wiring layer, the lowermost wiring layer and the first and second wiring layers are metal layers.

36. (previously presented) A semiconductor device comprising:

a semiconductor substrate;

a first wiring layer having a first thickness and provided above the semiconductor substrate; and

a second wiring layer having a second thickness thinner than the first thickness and provided above the first wiring layer,

wherein the first wiring layer comprises a first area having signal lines and a second area having power source lines, and a width of each of the power sources lines is greater than that of the signal lines.

37. (previously presented) A semiconductor device according to claim 36, further comprising:

a lowermost wiring layer nearest to the semiconductor substrate and provided below the first wiring layer; and

an uppermost wiring layer farthest from the semiconductor substrate and provided above the second wiring layer.

38. (previously presented) A semiconductor device according to claim 36, wherein a wiring pitch of the first wiring layer is greater than that of the second wiring layer.

39. (previously presented) A semiconductor device according to claim 36, wherein the first wiring layer is a layer on which a power source line is formed.

40. (previously presented) A semiconductor device according to claim 36, wherein the first wiring layer is substantially as thick as the uppermost wiring layer.

41. (previously presented) A semiconductor device according to claim 36, wherein the second wiring layer is substantially as thick as the lowermost wiring layer.

42. (previously presented) A semiconductor device according to claim 36, wherein all of the uppermost wiring layer, the lowermost wiring layer and the first and second wiring layers are metal layers.

43. (previously presented) A semiconductor device comprising:

a semiconductor substrate;

an IP core area on the semiconductor substrate;

a peripheral area on the semiconductor substrate except for the IP core area;

a first wiring layer having a first thickness and provided above the semiconductor substrate in the IP core area; and

a second wiring layer having a second thickness smaller than the first thickness and provided above the first intermediate wiring layer in the IP core area,

wherein the first wiring layer comprises a first area having signal lines and a second area having power source lines, and a width of each of the power source lines is greater than that of the signal lines.

44. (previously presented) A semiconductor device according to claim 43, further comprising:

a lowermost wiring layer nearest to the semiconductor substrate and provided below the first wiring layer; and

an uppermost wiring layer farthest from the semiconductor substrate and provided above the second wiring layer.

45. (previously presented) A semiconductor device according to claim 43, wherein the first wiring layer is a layer on which a core power source line is formed.

46. (previously presented) A semiconductor device according to claim 43, wherein a wiring pitch of the first wiring layer is greater than that of the second intermediate wiring layer.

47. (previously presented) A semiconductor device according to claim 43, wherein the first wiring layer is substantially as thick as the uppermost wiring layer.

48. (previously presented) A semiconductor device according to claim 43, wherein the second wiring layer is substantially as thick as the lowermost wiring layer.

49. (previously presented) A semiconductor device according to claim 43, wherein all of the uppermost wiring layer, the lowermost wiring layer and the first and second wiring layers are metal layers.

50. (currently amended) A semiconductor device comprising:

a semiconductor substrate;

a first wiring layer having a first thickness, extending in a direction parallel to a surface of the semiconductor substrate, and provided above the semiconductor substrate;

a second wiring layer having a second thickness greater than the first thickness, extending in the direction, and provided between the semiconductor substrate and the first wiring layer; and

a third wiring layer having a third thickness greater than the first thickness, extending in the direction, and provided above the first wiring layer;

wherein the first wiring layer comprises a first area having signal lines and each of the second and third wiring layers comprise a second area having power source lines, and a pitch of the power source lines is greater than that of the signal lines.

51. (currently amended) A semiconductor device comprising:

a semiconductor substrate;

a first wiring layer having a first thickness, extending in a direction parallel to a surface of the semiconductor substrate, and provided above the semiconductor substrate;

a second wiring layer having a second thickness smaller than the first thickness, extending the direction, and provided between the semiconductor substrate and the first wiring layer; and

a third wiring layer having a third thickness smaller than the first thickness, extending in the direction, and provided above the first wiring layer;

wherein the first wiring layer comprises a first area having power source lines, and each of the second and third wiring layers comprise a second area having signal lines, and a pitch of the power source lines is greater than that of the signal lines.